**CLAIMS:**

What is claimed is:

1. A method in a data processing system for managing direct memory access transfers, the method comprising:

monitoring for an event to pass a new thread ownership to a direct memory access resource; and

responsive to detecting the event, adding a buffer of the new thread to an end of a direct memory access chain of requests for the current thread to generate a direct memory access request, wherein adding the buffer to the end of a direct memory access chain provides an anchor point for the new thread to add additional requests for the direct memory access resource.

2. The method of claim 1, wherein the direct memory access request is a zero transfer length direct memory access request.

3. The method of claim 1, wherein the monitoring step and the adding step are performed by an operating system.

4. The method of claim 3, wherein the buffer is in a memory location for the new thread.

5. The method of claim 1, wherein the event is a selected period of time.

6. The method of claim 1, wherein the direct memory access resource is at least one of a graphics adapter, a communications adapter, and a hard disk drive.

7. The method of claim 1, wherein the new thread is in a sleep mode and further comprising:

waking the new thread from the sleep mode to pass ownership of the direct memory access resource to the new thread.

8. A direct memory access control system comprising:

a direct memory access engine, wherein the direct memory access engine processes a chain of requests and accepts requests from user level threads; and

a direct memory access control component, wherein the direct memory access control component grants access to the direct memory access engine a single thread at a time, detects an event to transfer access to the direct memory access engine from a first thread to a second thread, links a selected buffer from a buffer pool of the second thread to a last buffer in the chain of requests in response to detecting the event, wherein the buffer provides the second thread access to the direct memory access engine.

9. The method of claim 8, wherein the selected buffer has a length set equal to zero causing the direct memory access engine to ignore the buffer and wherein the selected buffer provides an addressable anchor point for

the second thread to chain requests for the second thread.

10. A data processing system for managing direct memory access transfers, the data processing system comprising:

a bus system;

a communications unit connected to the bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit executes the set of instructions to monitor for an event to pass a new thread ownership to a direct memory access resource; and add a buffer of the new thread to an end of a direct memory access chain of requests for the current thread to generate a direct memory access request in which adding the buffer to the end of a direct memory access chain provides an anchor point for the new thread to add additional requests for the direct memory access resource in response to detecting the event.

11. A data processing system for managing direct memory access transfers, the data processing system comprising:

monitoring means for monitoring for an event to pass a new thread ownership to a direct memory access resource; and

adding means, responsive to detecting the event, for adding a buffer of the new thread to an end of a direct memory access chain of requests for the current thread to generate a direct memory access request, wherein adding

the buffer to the end of a direct memory access chain provides an anchor point for the new thread to add additional requests for the direct memory access resource.

12. The data processing system of claim 11, wherein the direct memory access request is a zero transfer length direct memory access request.

13. The data processing system of claim 11, wherein the monitoring means and the adding means are performed by an operating system.

14. The data processing system of claim 13, wherein the buffer is in a memory location for the new thread.

15. The data processing system of claim 11, wherein the event is a selected period of time.

16. The data processing system of claim 11, wherein the direct memory access resource is at least one of a graphics adapter, a communications adapter, and a hard disk drive.

17. The data processing system of claim 11, wherein the new thread is in a sleep mode and further comprising:

waking means for waking the new thread from the sleep mode to pass ownership of the direct memory access resource to the new thread.

18. A computer program product in a computer readable medium for managing direct memory access transfers, the computer program product comprising:

first instructions for monitoring for an event to pass a new thread ownership to a direct memory access resource; and

second instructions, responsive to detecting the event, for adding a buffer of the new thread to an end of a direct memory access chain of requests for the current thread to generate a direct memory access request, wherein adding the buffer to the end of a direct memory access chain provides an anchor point for the new thread to add additional requests for the direct memory access resource.